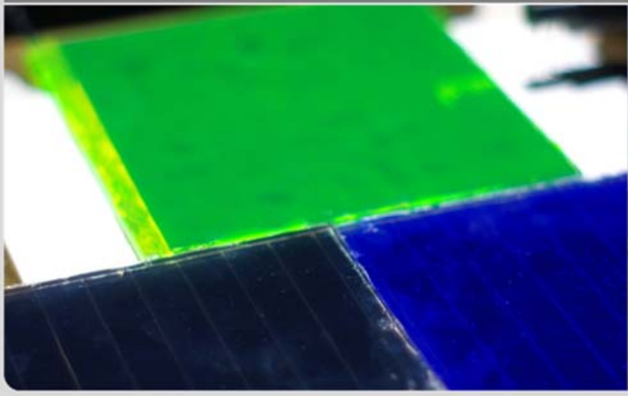
"Solar Energy" WS 2014/2015

Lecture 7:
Part 1: Fabrication of Silicon Solar Cells
Part 2: Thin Film Crystalline Silicon Solar Cells

Prof. Dr. Bryce S. Richards

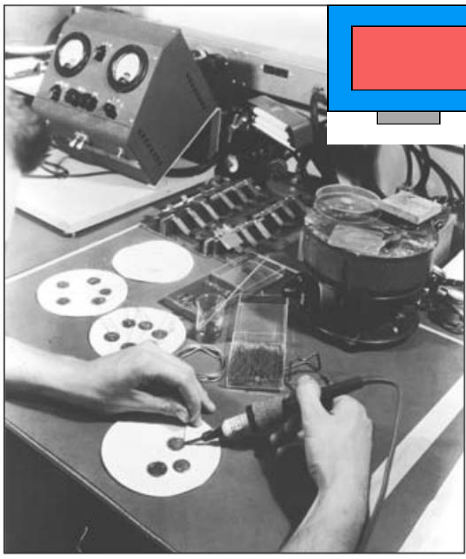
Institute of Microstructure Technology (IMT), Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen
Light Technology Institute (LTI), Engesserstrasse 13, Building 30.34, 76131 Karlsruhe

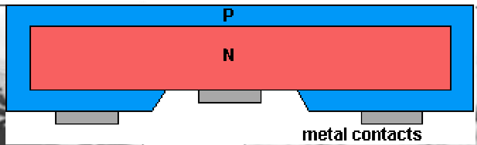
KIT Focus Optics & Photonics

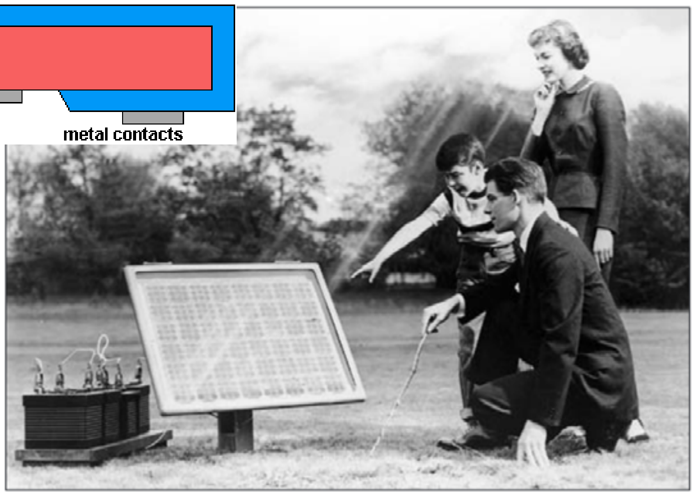


Silicon – Long History

Forefather of today's Si solar cell date to 1954 by researchers at Bell Laboratories (USA). Cells had a diffused junction and both *n*- and *p*-type contacts on the rear ⇒ η = 6% (15x that of earlier devices). First application for space ⇒ remained major market until early 1970's



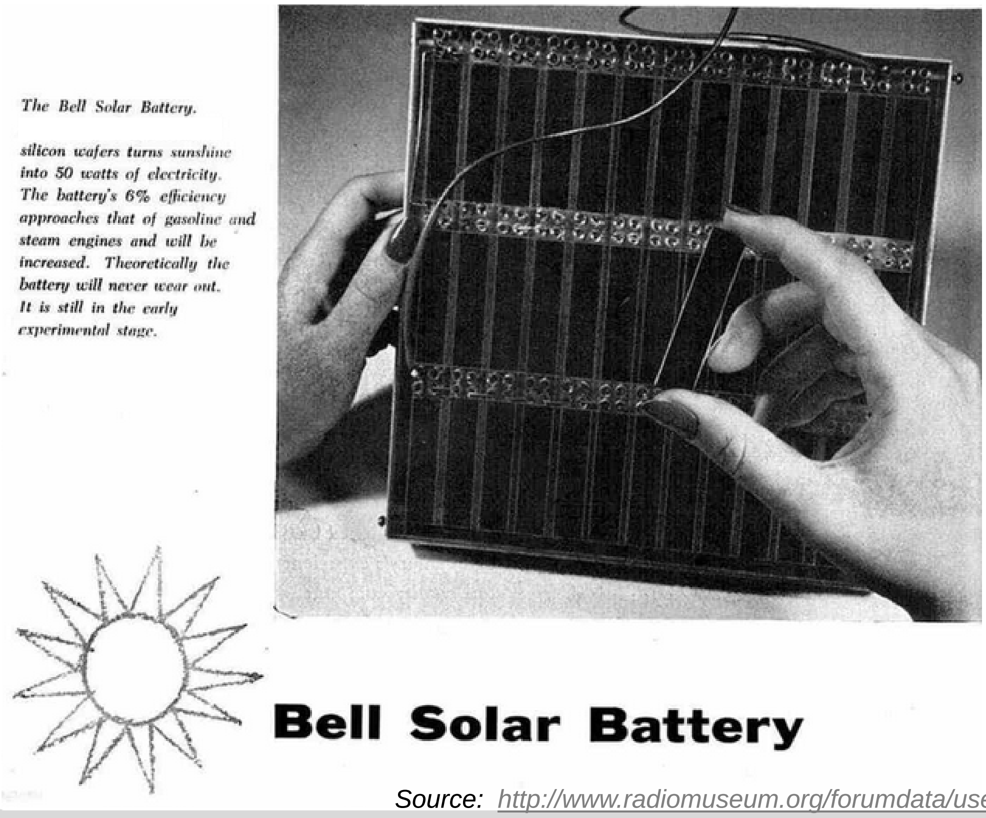




Advertisement photos, such as this one that appeared in the 1956 issue of Look Magazine, show off the "Bell Solar Battery" to the American public.

Source: http://www.pveducation.org/pvcdrom/manufacturing/early-silicon-solar-cells
http://www.nrel.gov/education/pdfs/educational_resources/high_school/solar_cell_history.pdf

Silicon – Long History



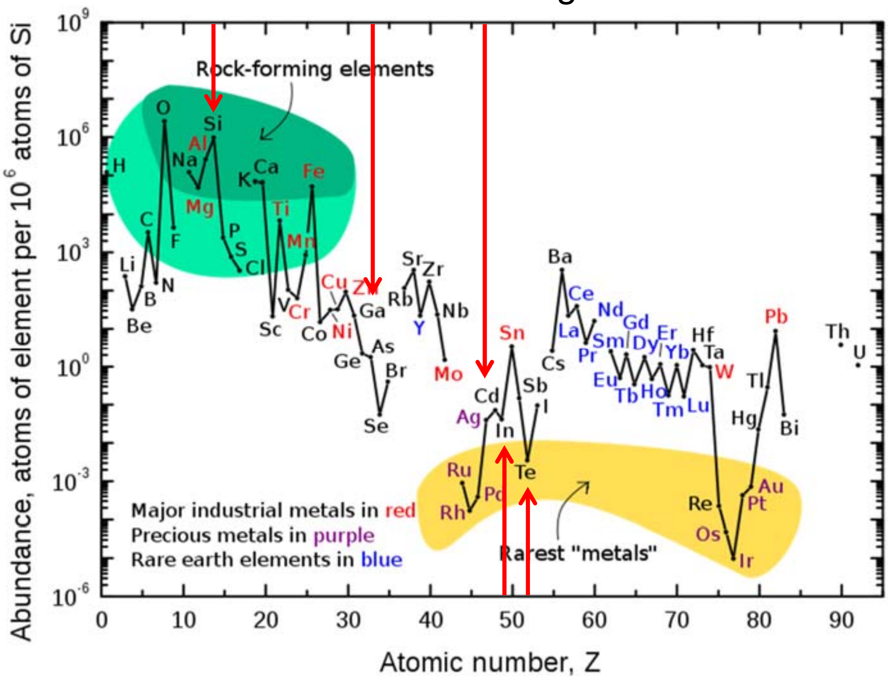
Source: http://www.radiomuseum.org/forumdata/users/6435/Cxt/07_cell.jpg

Refining Silicon

Silicon dioxide (SiO_2) ⇒ most abundant mineral in earth's crust ⇒ manufacture of hyperpure silicon for PV occurs in two stages

1. Oxygen is removed to produce metallurgical grade silicon
2. Further refined to produce electronic grade silicon

An intermediate grade with impurity levels between 1) and 2) above is often termed solar grade silicon



Source: http://en.wikipedia.org/wiki/Abundance_of_the_chemical_elements

Metallurgical Grade Silicon

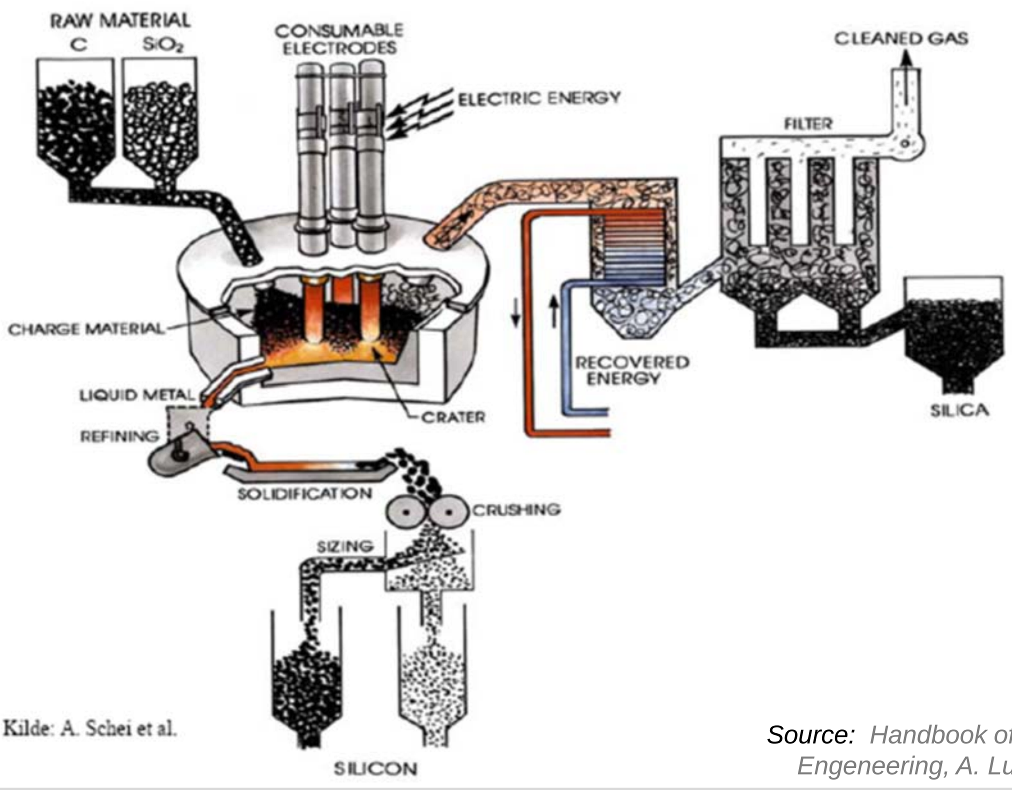
Silica (SiO_2) occurs naturally as quartz. Most common raw material for electronic grade is high purity quartz rock, but could also use beach sand. Ideally, silica has low concentrations of Fe, Al and other metals.

Silica reduced (oxygen removed) through reaction with carbon (coal, charcoal) and heating to 1500-2000 °C in an electrode arc furnace

$$SiO_2 + C \rightarrow Si + CO_2$$

Result is metallugical grade silicon (MG-Si)
$\Rightarrow$ 98% pure and used extensively in the metallurgical industry

Metallurgical Grade Silicon



Source: Handbook of PV Science and Engeneering, A. Luque, Wiley, 1998

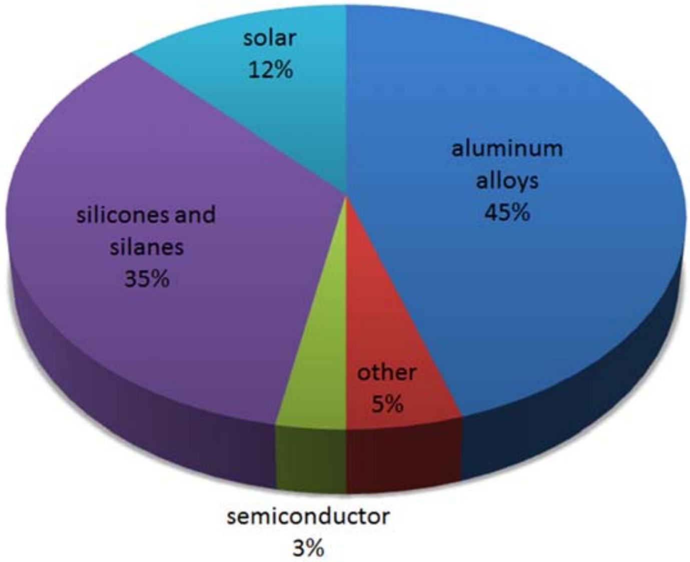
Metallurgical Grade Silicon

In 2013 the total production of silicon was 7.6 million tonnes. Low cost of few $/kg with an energy content of 14–16 kWh/kg

Solar industry consumes 4x as much as silicon as remainder of semiconductor industry

N.B. differences between

- silicon
- silica
- silicone…!



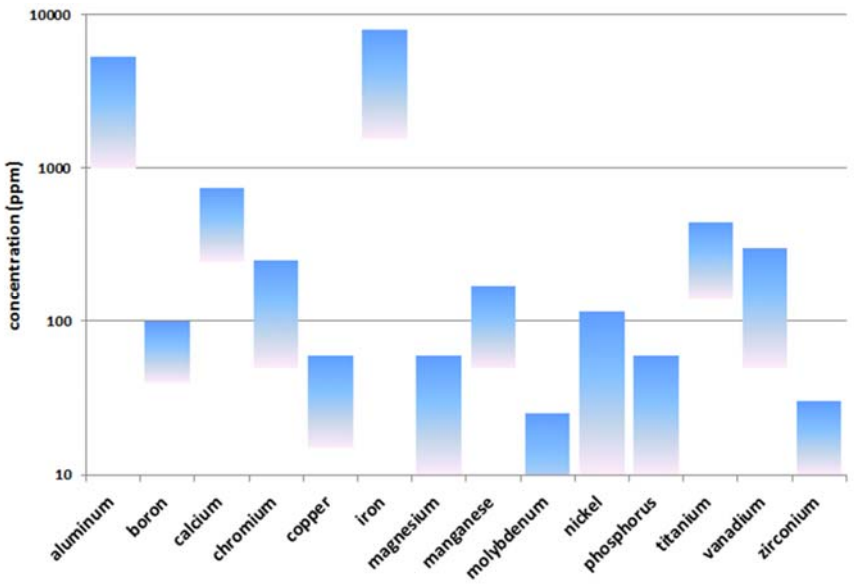
Source: http://www.pveducation.org/pvcdrom/manufacturing/refining-silicon

Metallurgical Grade Silicon

2% impurities are mainly carbon, alkali-earth and transition metals and hundreds of ppm of B and P

Transition metals in silicon result in deep levels in bandgap ⇒ high recombination activity makes MG-Si unsuitable for use in electronics

Also, the B and P dopant concentrations are way too high (we need ppb)



Source: http://www.pveducation.org/pvcdrom/manufacturing/refining-silicon

Metallurgical Grade Silicon

Extensive research in ~1980s determining the effect of impurities on solar cell efficiency

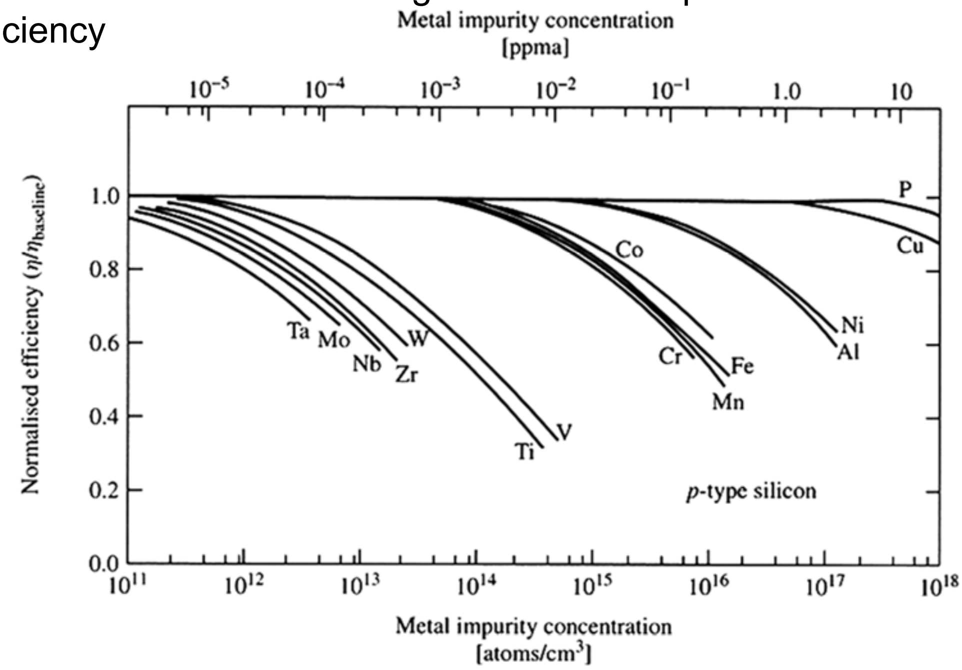


Figure 5.11 Solar cell efficiency versus impurity concentration for 4 ohm cm p-base devices [30]. Reproduced from Davis Jr. J *et al.*, *IEEE Trans. Electron Devices* © 1980 IEEE

Electronic Grade Silicon

Small amount of MG-Si further refined for semiconductor industry. Powdered MG-Si reacted with anhydrous HCl at 300 °C in a fluidized bed reactor to form trichlorosilane ($SiHCl_3$)

$$Si + 3HCl \rightarrow SiHCl_3 + H_2$$

Impurities such as Fe, Al, and B react to form halides (e.g. $FeCl_3$, $AlCl_3$,…). $SiHCl_3$ has low boiling point of 31.8 °C ⇒ distillation used to purify $SiHCl_3$ from impurity halides ⇒ now has < 1 ppb of electrically active impurities.

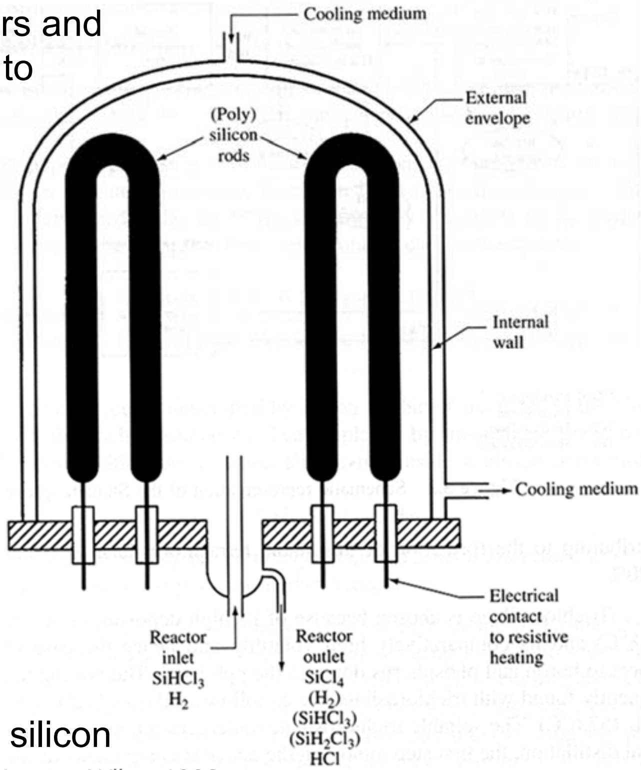
Finally, pure $SiHCl_3$ reacts with hydrogen at 1100°C for ~200 – 300 hours to produce a very pure silicon

$$SiHCl_3 + H_2 \rightarrow Si + 3\,HCl$$

Electronic Grade Silicon (EG-Si)

Reaction inside large vacuum chambers and Si deposited onto thin polysilicon rods to produce high-purity polysilicon (~Ø200mm). "Siemens process" first developed 1960's

Rods of EG-Si then broken ⇒ form feedstock for crystallisation process

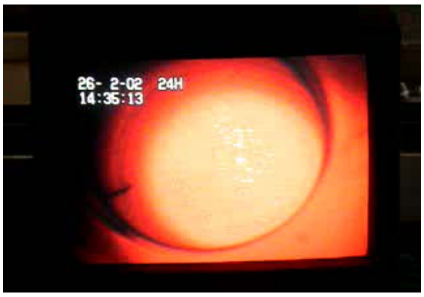


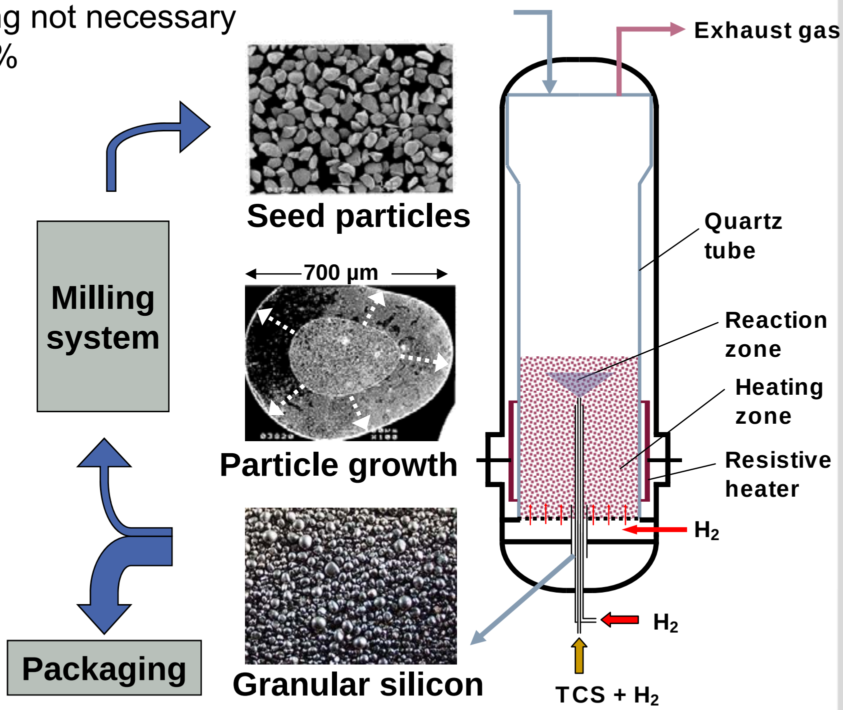
Production requires a lot of energy. Solar cells can tolerate higher levels of impurities than for IC fabrication
⇒ proposals for creating "solar-grade" silicon

Source: Handbook of PV Science and Engeneering, A. Luque, Wiley, 1998

Solar Grade Silicon

Fluidized bed granular deposition – continuous process of CVD of poly-Si
Advantages: milling and etching not necessary
⇒ Cost reduction potential 25%





WACKER POLYSILICON

Source: Schulze, PV Crystallox, Wacker

Solar Grade Silicon

In this continuous process, silicon is deposited from $SiHCl_3$ on Si seed crystals (Ø0.3 – 0.7 mm) ⇒ specific surface area greater than silicon rod in Siemens process

Granules of poly-silicon then continuously "harvested" from the reactor

The fluidized bed process is economic for "solar" poly-silicon for several reasons:

- deposits more silicon in the same time than Siemens process
- reduced electrical heating power
- reactor doesn't need to be cooled to open to remove silicon
- eliminates the costly accidental breakage of rods
- granules also better suited for further processing

⇒ so far SG-Si only used in the development and pilot production

Single Crystal Silicon

Czochralski (Cz) process ⇒ most commonly used by both solar IC industry to produce single crystal ingot (process shown below). The use of quartz crucibles in manufacture of Cz Si results in
⇒ incorporation of ppm (10^{18} cm^{-3}) of O into Si ingot
⇒ creates complex with B dopant that degrades *L* over time (does not happen in *n*-type ingots fabricated with phosphorus)

Rejected "tops" and "tails" from IC industry recycled into solar industry

Energy content of Cz c-Si ~210 kWh per kg of EG-Si

Source: http://www.pveducation.org/pvcdrom/manufacturing/czochralski-silicon

Single Crystal Silicon

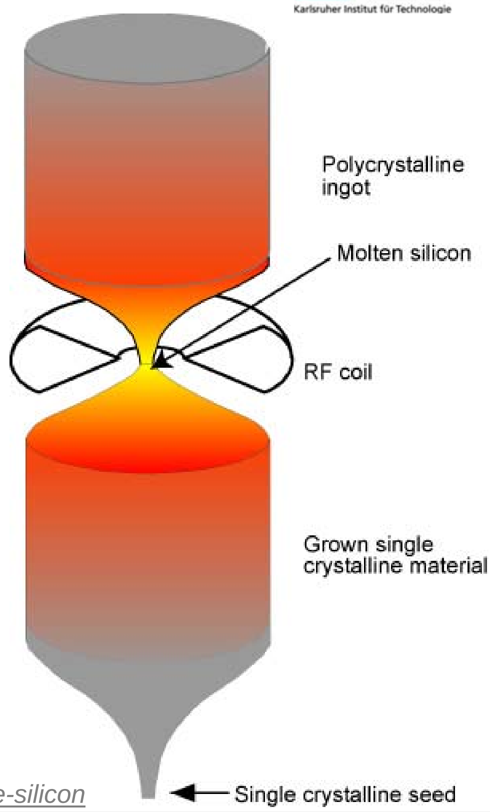
Source: http://www.pveducation.c
manufacturing/czochralsk

Single Crystal Silicon

To avoid B-O complex or for other ultra-pure silicon ⇒ use float zone (FZ) process instead

Process: molten region is slowly passed along rod of silicon ⇒ impurities tend to stay in molten region rather than be incorporated into solidified region ⇒ allows a very pure single crystal region to remain after the molten region has passed

Due to the difficulty in growing large diameter ingots and the often higher cost, FZ wafers typically only used for laboratory cells and are less common in commercial production



Source: http://www.pveducation.org/pvcdrom/manufacturing/float-zone-silicon

Multi-Crystalline Silicon

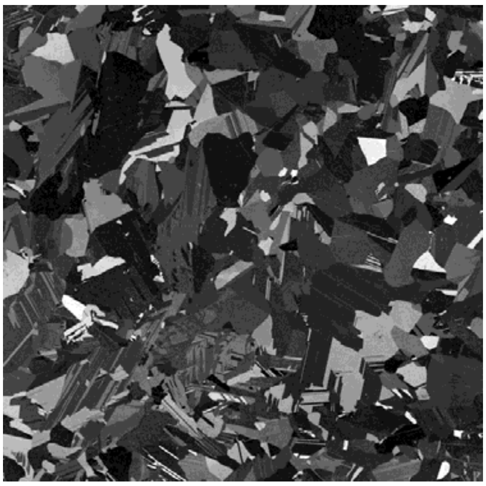
Can also produce multicrystalline silicon (mc-Si) which is
- ☑ simpler,
- ☑ less energy intensive (8-15 kWh/kg), and
- ☑ cheaper, but…
- ☒ … lower quality material due to presence of grain boundaries

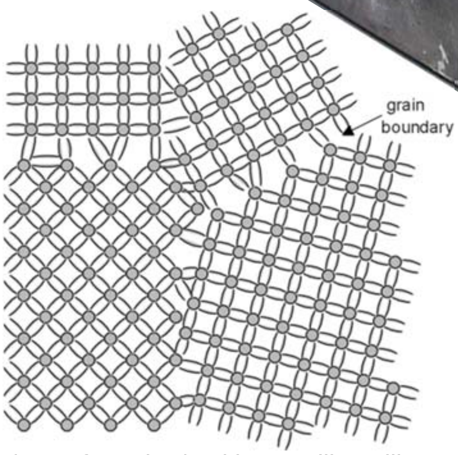
Grain boundaries introduce
- high localised regions of recombination due to introduction of extra defect energy levels into bandgap ⇒ reduces *L*
- Barriers to flow of carriers and providing shunting paths for current flow across *p-n* junction

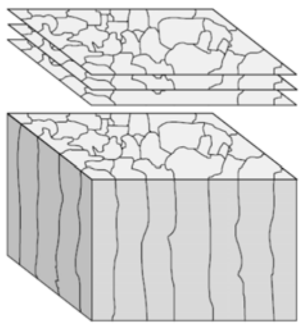
Source: http://www.pveducation.org/pvcdrom/manufacturing/float-zone-silicon

Multi-Crystalline Silicon

To avoid significant recombination losses, grain sizes of ≥ mm are required ⇒ also allows single grains to extend from front to back of the cell, providing less resistance to carrier flow



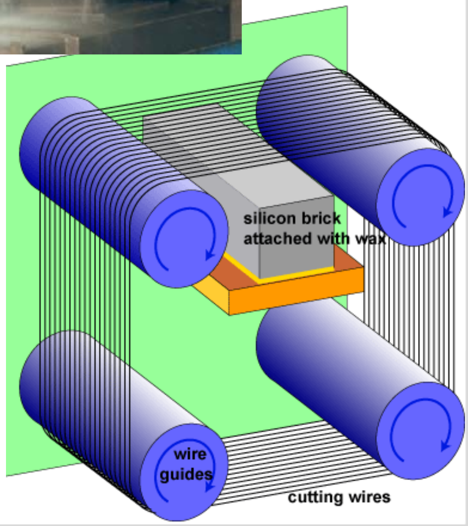




Source: http://www.pveducation.org/pvcdrom/manufacturing/multi-crystalline-silicon

Wafer Slicing

Once ingot is grown ⇒ then sliced up into wafers. For mc-Si, large slabs are then sliced up first into smaller "bricks" using diamond saw. Wafers then realised using a wire saw with SiC slurry

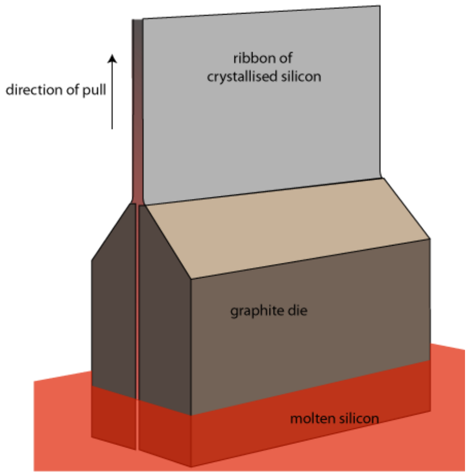


Source: http://www.pveducation.org/node/496

Wafer Slicing

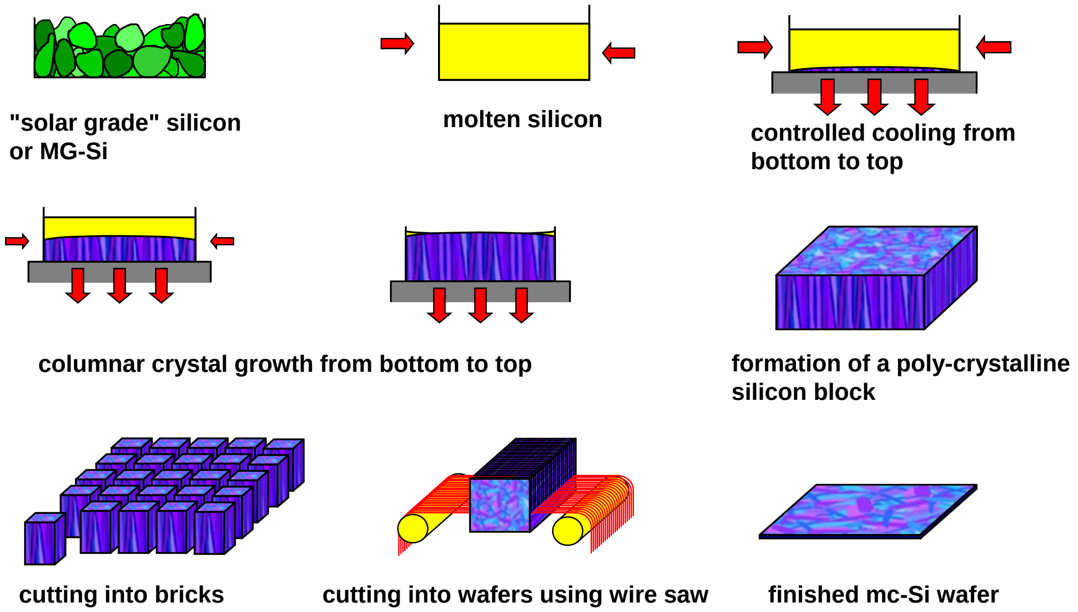
The "kerf" losses due the sawing can be high ⇒ other processes investigated to grow wafers from the outset ⇒ avoid cutting process

<u>Edge Defined Film Fed Growth (EFG)</u> technique uses a die to define thickness of a silicon sheet. Careful adjustment of the temperature profile of graphite die causes the Si sheets to crystallize with large grains.



Source: http://www.pveducation.org/pvcdrom/manufacturing/other-wafering-techniques

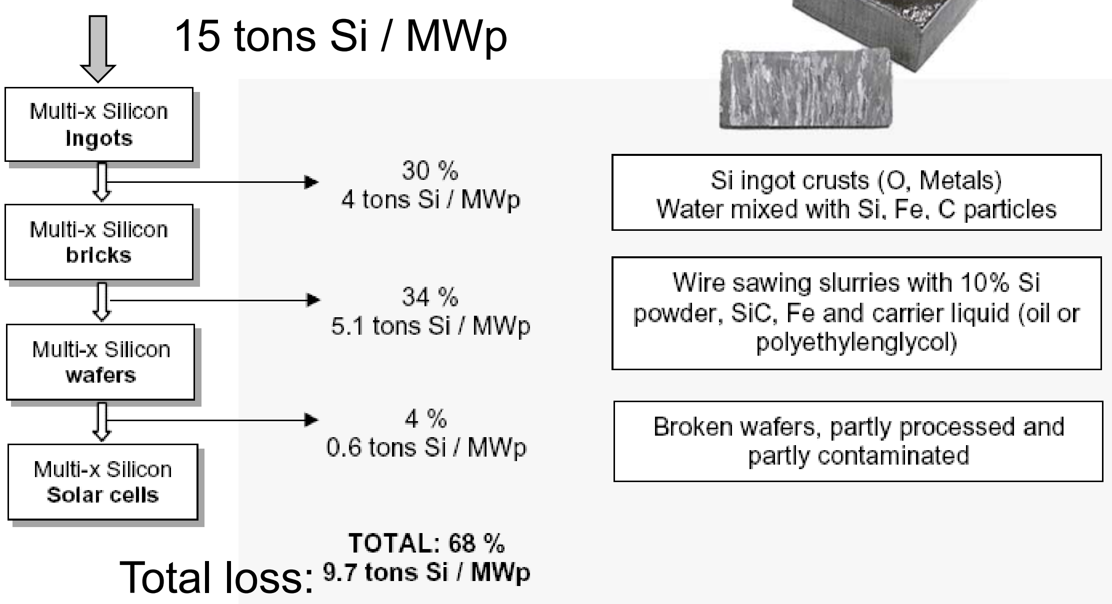
Production of mc-Si Wafers



Source: *C.Gerhards, Dissertation, Konstanz 2002, U.Kindereit, Studienarbeit, Berlin 2004)*

Losses in the Wafer Process

15 tons Si / MWp



Total loss: 9.7 tons Si / MWp

Total of 5.3 tons (32%) goes into solar cells

Source: *D. Sarti and R. Einhaus, Photowatt (2002)*

Solid State Diffusion

Process for introducing dopant atoms into semiconductors. In Si solar cell processing, typically start with a uniformly doped *p*-type wafer (the “base”). The *n*-type emitter layer is formed through phosphorus doping

Source: http://www.pveducation.org/pvcdrom/manufacturing/solid-state-diffusion

Solid State Diffusion

The diffusion process follows Fick's law:

$$j = -D\frac{\partial N}{\partial x}$$

where

j = flux density (atoms cm^{-2}),

D = diffusion coefficient ($cm^2\,s^{-1}$)

N = concentration volume (atoms cm^{-3})

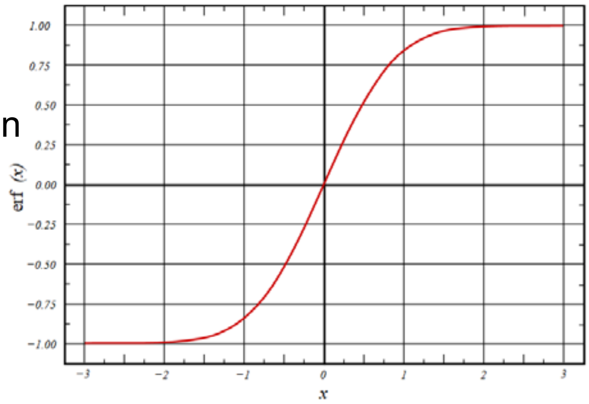
x = distance (cm)

Typically, what happens is that the Si wafer is placed in a furnace with unlimited source (e.g. phosphorus saturated carrier gas), and then turning off the source and driving in the phosphorus atoms further into the wafer

Source: http://www.pveducation.org/pvcdrom/manufacturing/solid-state-diffusion

Solid State Diffusion

Diffusion from an Unlimited Source:
to produce a shallow junction with a very high surface concentration of P atoms, described by complementary error function



$$N(x,t) = N_0 erfc \frac{x}{2\sqrt{Dt}}$$

where
N_0 = impurity concentration at surface (atoms cm^{-3})
t = time (sec)

Simple one-step diffusion is useful where there is no surface passivation of the device.

Source: http://en.wikipedia.org/wiki/Error_function

Solid State Diffusion

Diffusion from a Limited Source: consists of two-step process

1. a short pre-deposition as outlined above, followed by
2. a longer drive-in at a higher temperature to provide a deep and lightly-doped emitter

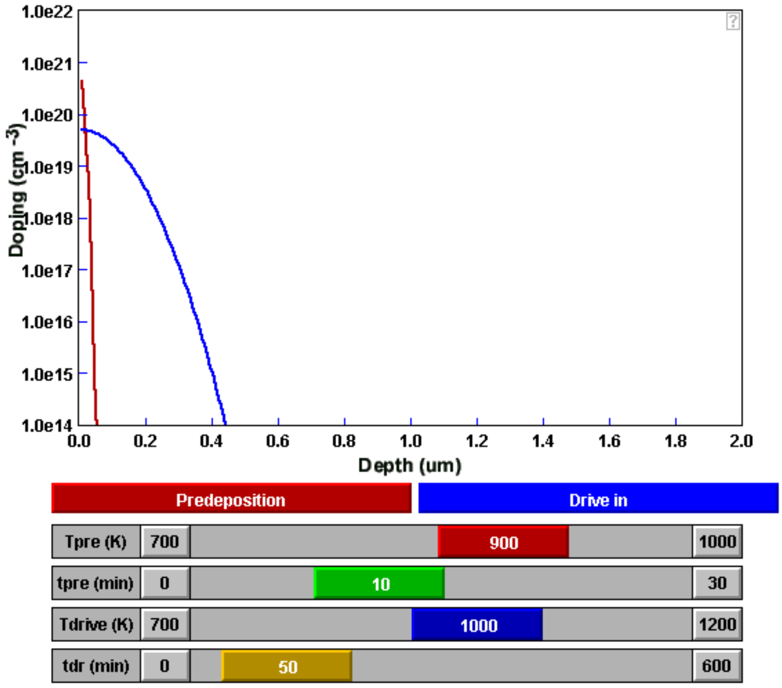
If the drive-in is at a higher temperature the final profile is a Gaussian, described by:

$$N(x,t) = \frac{Q_0}{\sqrt{\pi D t}} e^{-\left(\frac{x}{2}\sqrt{Dt}\right)^2}$$

where
Q_0 = is atoms introduced in the pre-deposition (atoms cm^{-2})

Solid State Diffusion

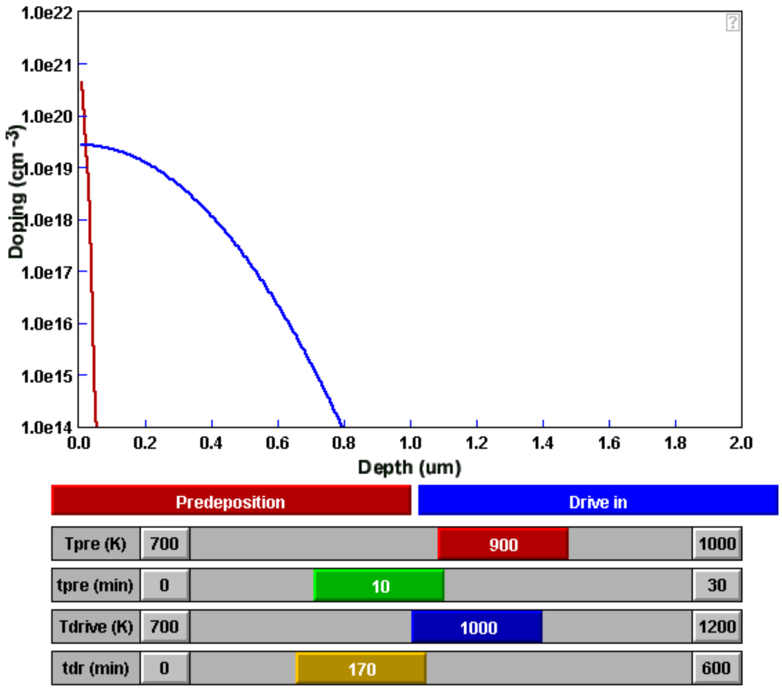
Pre-dep: 900°C for 10min
Drive-in: 1000°C for 50min



Source: http://www.pveducation.org/pvcdrom/manufacturing/solid-state-diffusion

Solid State Diffusion

Pre-dep: 900°C for 10min
Drive-in: 1000°C for 170min



Source: http://www.pveducation.org/pvcdrom/manufacturing/solid-state-diffusion

Screen Printed Solar Cells

Screen-printed solar cells first developed in 1970's ⇒ most mature solar cell fabrication technology ⇒ currently dominate the market for terrestrial PV. Key advantage of screen-printing is the simplicity of process. Basic process in animation below (since improved upon by many manufacturers and research laboratories)

Summary animation:

Source: *http://www.pveducation.org/pvcdrom/manufacturing/screen-printed*

Screen Printed Solar Cells

Fabrication sequence:

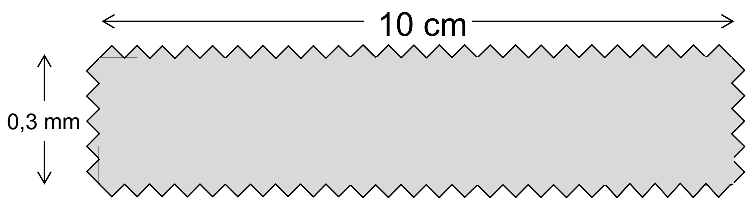
1. Sawing
   of monocrystalline or mc-Si ingots to produce wafers
2. Etching
   to remove saw damage (20µm from either side of wafer etched off)
3. Texturing (only for mono-Si)
   <100> oriented Si wafers are textured, results in exposing the <111> crystal planes as pyramids 1-10µm high using KOH-based etch
4. Emitter diffusion
   typically performed as phosphorus diffusion to achieve *n*-type emitter in a p-type (boron-doped) substrate. Conducted in a tube furnace at about 900°C. Followed by i) plasma etching of the undesired junction around the edge and ii) etching off the phosphorus glass (P_2O_5)

Screen Printed Solar Cells

5. Passivation and ARC
   the most common material used as an ARC (a-SiN_x:H) can also afford some passivation of surface and bulk defects (via
6. Printing
   of pastes – contain metal particles (5-10 µm Ag oder Al) as well as glass frit to help etch through the SiN_x layer
7. Firing
   of pastes at high T, with the glass frit also improving adhesion.
   Advantages of screen printing: higher metal yield
   Disadvantages: - Grids can't be smaller than 100µm
   - Particle nature of metal limits conductivity
   ⇒ but still the standard process in industry
   ⇒ steps 6. und 7. are repeated twice – once for back contact and once for the front contact
8. Measurement under "solar simulator" and sorting

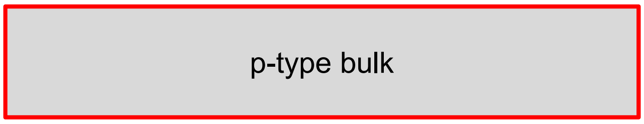
Additional step: Al or B doped BSF sometimes performed

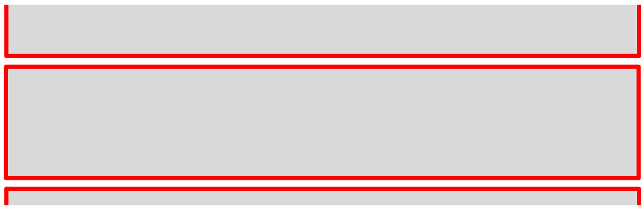
p-type (1 × 16 B atoms/cm³) wafer
with ~300 µm thickness.



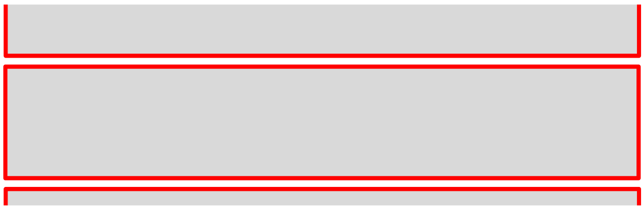
Etching away the saw damage

p-n junction formation in
phosphorus-containing atmosphere
at ~900°C



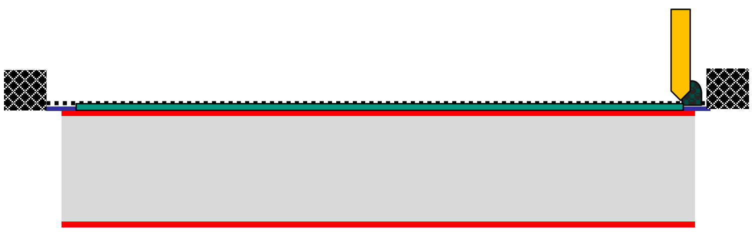


Cells stacked on top of each other for
edge isolation
Reactive plasma etching



Screen printing of rear contact
A maske is laid on top of the wafer and
an Al and/or Ag paste …

… is pressed through the mask.



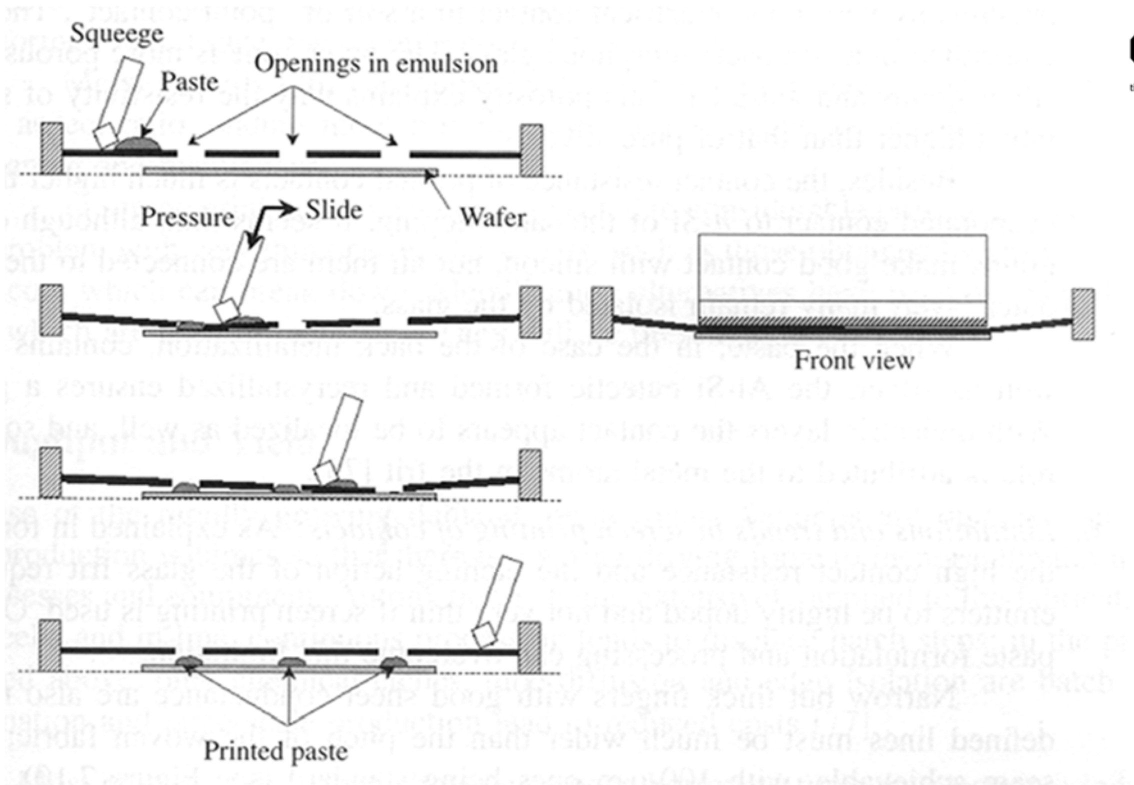
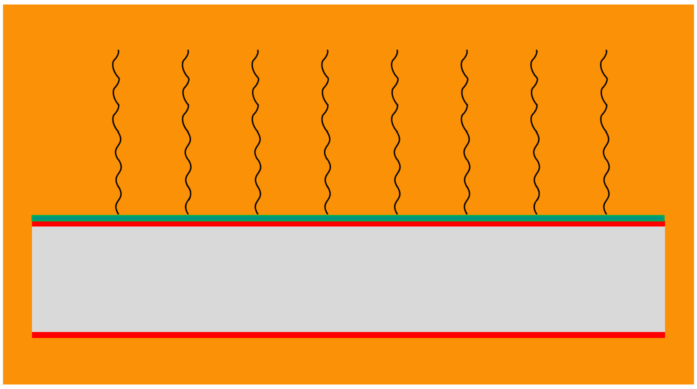


Figure 7.9 Illustration of a printing sequence

Source: Handbook of PV Science and Engineering, Luque, Wiley

The mask is removed and the remaining wet metal paste is dried in an furnace.

The organic binding material is evaporated off

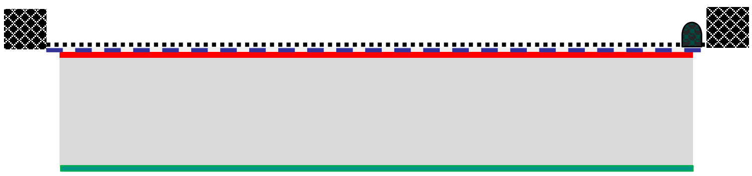


At higher temperatures, contact between the metal and silicon is made (diffusion)

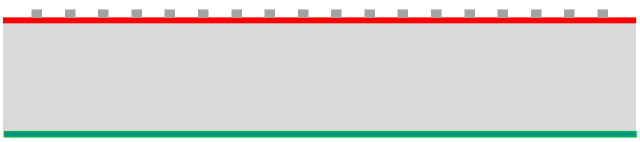
Which converts the rear n-type layer to p-type

The cell is now turned over to the front side

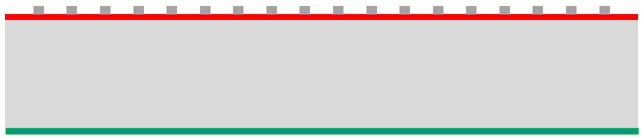
Front contact is produced in a similar way to the rear, but with a different mask that specifies the desired grid contact

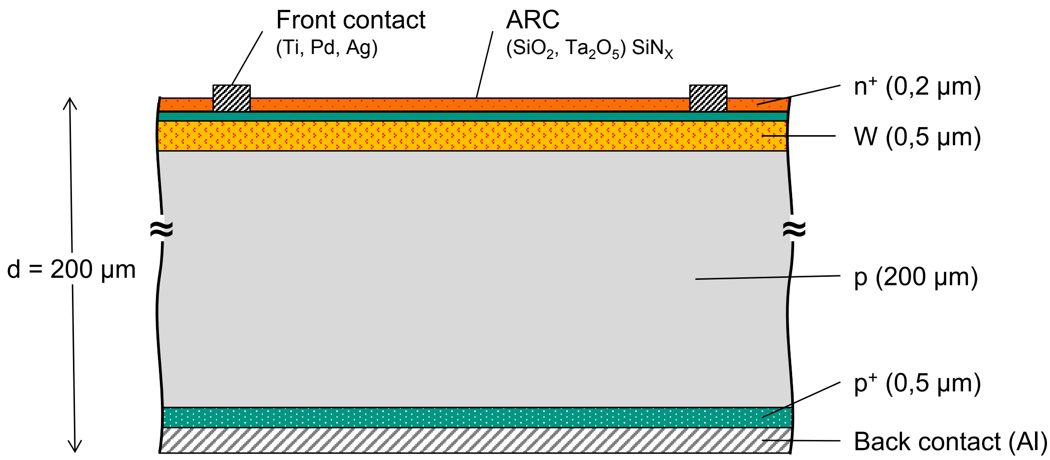


Hopefully low shading is achieved and this grid pattern is now fired



We now have a finished solar cell





Screen Printed Solar Cells

Many variations to animation shown above, which give higher efficiencies, lower costs or both. Some of these specific techniques described below

Phosphorus Diffusion:

Screen-printed solar cells typically use a simple homogeneous diffusion (x-y direction) to form the emitter ⇒ doping is same beneath metal contacts and between fingers.

To maintain low contact resistance (R_S), a high surface concentration of P is required below the screen-printed contact. But, the high surface concentration of P produces a "dead layer" that reduces the EQE of the cell in the UV/blue region.

Developments: reduced R_S and improved blue response achieved via newer cell designs that

i) can contact shallower emitters

ii) possess “selective emitters” ⇒ with higher doping below the metal contacts have also been proposed (makes process more complicated as it involves a subsequent alignment step)

Phosphorus Diffusion: *p-n* junction formation

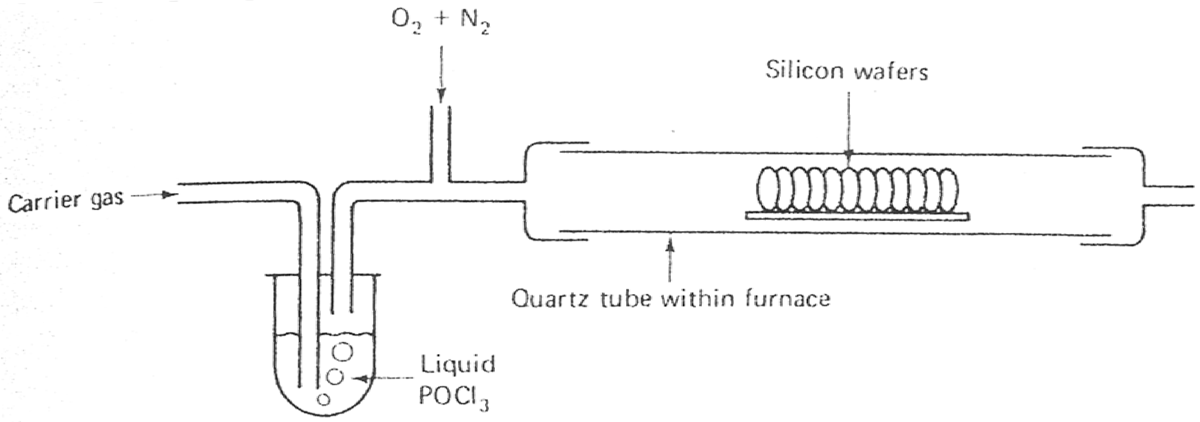


Figure 6.4. Phosphorus diffusion process.

- Evaporation of liquid $POCl_3$
- Transported via a carrier gas (N_2)
- Deposited as a P-doped glass layer (P_2O_5) onto wafer
- P_2O_5 is the diffusion source for P at high T ~900°C

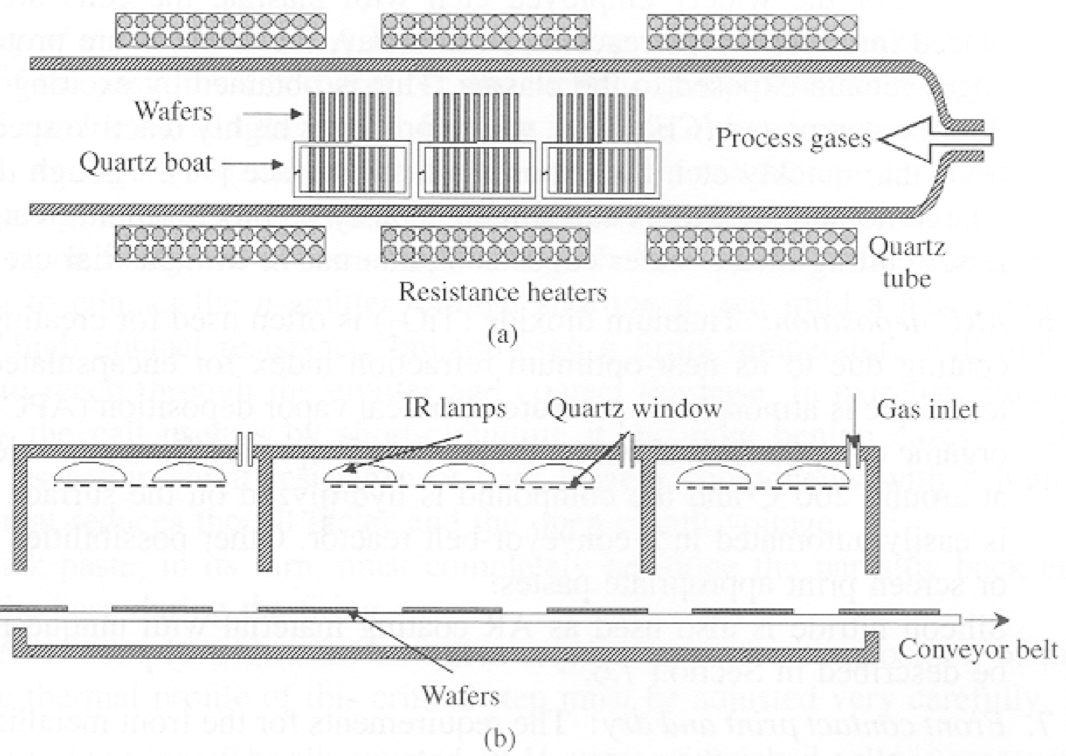


Figure 7.7 (a) A quartz furnace; and (b) a belt furnace for the diffusion of phosphorus

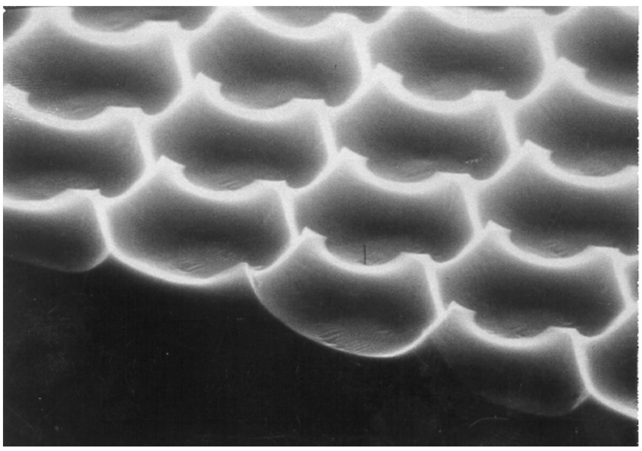
Source: *Handbook of PV Science and Engineering, Luque, Wiley*

Screen Printed Solar Cells

Surface Texturing to Reduce Reflection:
While monocrystalline Si wafers are easily textured with a NaOH or KOH based chemical etch to from pyramids and reduce reflection, same process is only marginally effective on the randomly orientated grains of mc-Si.

Various schemes have been proposed to texture mc-Si material:

- mechanical texturing of the wafer surface with cutting tools or lasers
- isotropic chemical etching based on defects rather than crystal orientation
- isotropic chemical etching in combination with a photolithographic mask →
- plasma etching



Source: *http://www.pveducation.org/pvcdrom/design/surface-texturing*

Screen Printed Solar Cells

Antireflection Coatings and Fire Through Contacts:
ARCs are particularly beneficial for mc-Si since it cannot be easily textured. Two common antireflection coatings are titanium dioxide (TiO_2) and silicon nitride (SiN_x). The coatings are applied through techniques like spraying or chemical vapour deposition (CVD). In addition to the optical benefits, dielectric coatings can also improve the electrical properties of the cell by surface passivation.

By screen-printing over the ARC with a paste containing cutting agents, the metal contacts can fire though the ARC and bond to the underlying silicon. This simplifies processing and has the added advantage of contacting shallower emitters

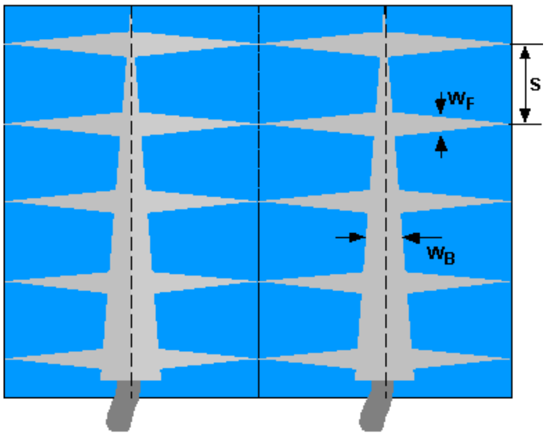
Edge Isolation
Various techniques have been investigated for edge isolation such as plasma etching, laser cutting, or masking the border to prevent diffusion from occurring around the edge in the first place

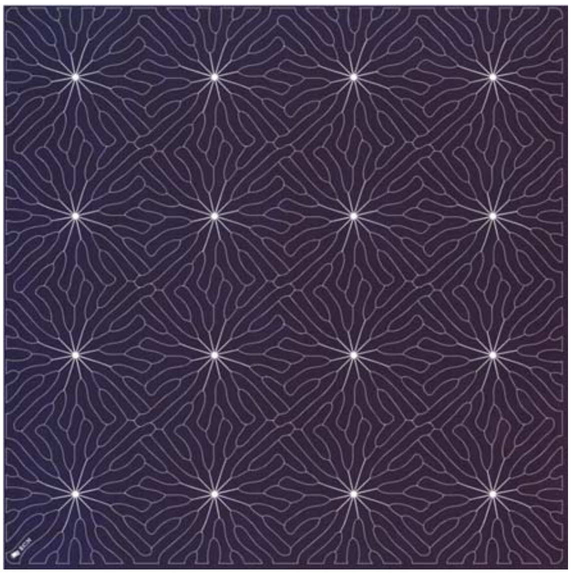
Screen Printed Solar Cells

Rear Contact
A full Al layer printed on the rear on the cell, with subsequent alloying through firing, produces a BSF and improves the cell bulk through “gettering” (a way of disabling the effect of impurities). However, the Al is expensive and a second print of Al/Ag is required for solderable contact. In most production, the rear contact is simply made using a Al/Ag grid printed in a single step.

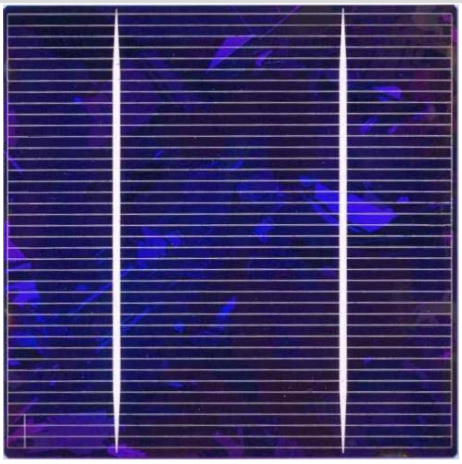
Substrate
Screen-printing has been used on a variety of substrates. The simplicity of the sequence makes screen-printing ideal for poorer quality substrates such as mc-Si as well as Cz. The general trend is to move to larger size substrates – now up to 15cm x 15cm for mc-Si and reduce the wafer thickness (e.g. down to 200 μm)

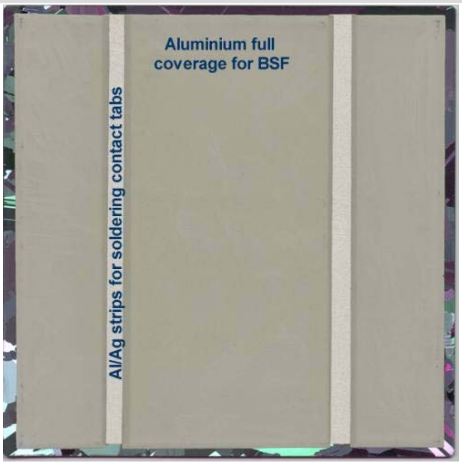
Screen Printed Solar Cells

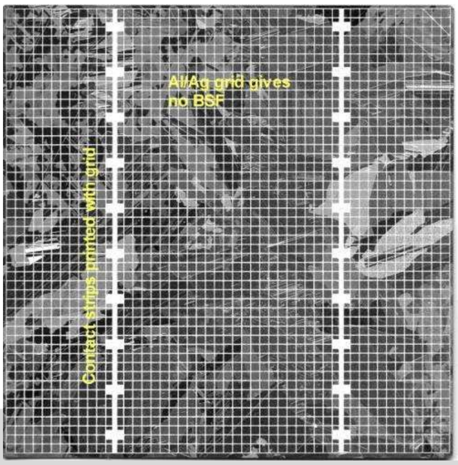


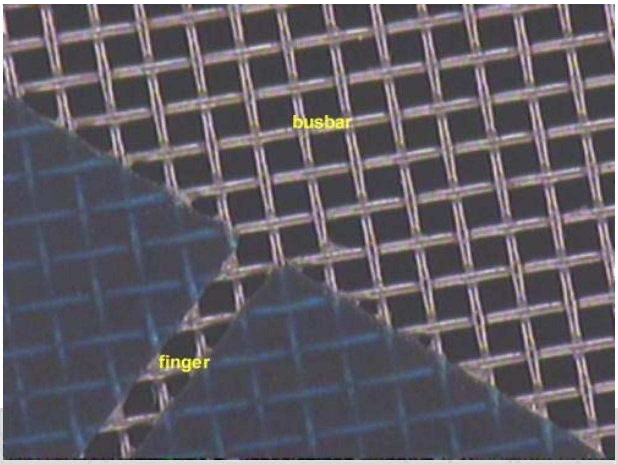


Grid design – traditional (left) or special for a rear-contact structured device



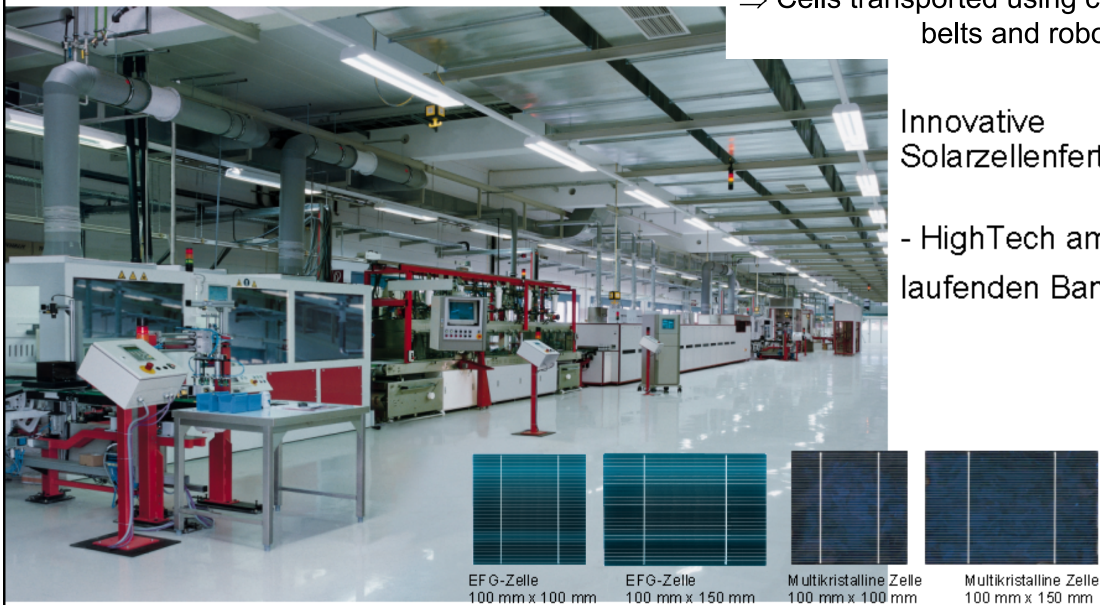






Produktionsanlage in Alzenau

Production line includes:
Cleaning, P-Diffusion, glass removal, ARC, back contact, front contact, measurement and inspection
⇒ Cells transported using conveyor belts and robots



Innovative Solarzellenfertigung

- HighTech am laufenden Band -

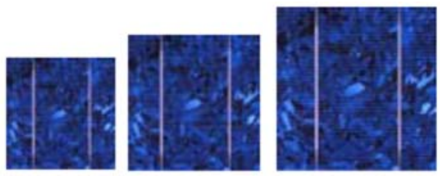
80m long
Process time 2.5h
5 parallel lines

RWE Solar GmbH 9

Movie

Screen Printed Solar Cells

Overview



Only one high-T step (P-diff. at 900°C)

Sintering of contacts needs only 400°C
→ relatively cheap
→ Surfaces has sub-optimal electrical and optical properties

Front:
low lifetime in highly-doped emitter region
poorly textured front surface has high reflectivity

Back:
high recombination at metal rear
resistive losses
optical losses via parasitic absorption at metall/Si interface and poor reflectance from rear side

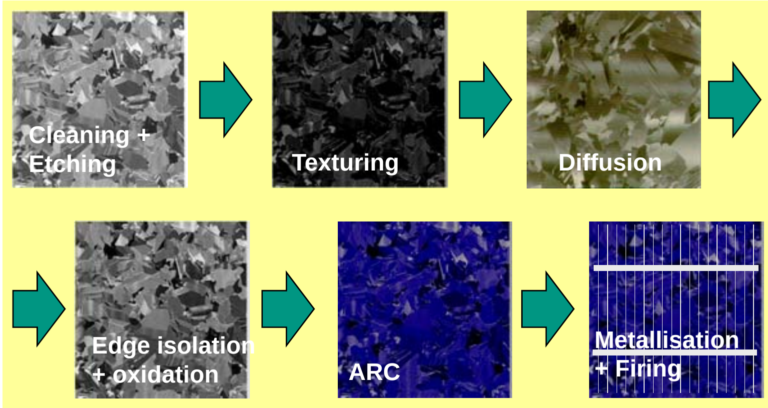
Size:

4 inch	100 x 100 mm²	$I_{sc} \sim 3.0$ A
5 inch	125 x 125 mm²	$I_{sc} \sim 4.9$ A
6 inch	156 x 156 mm²	$I_{sc} \sim 8.5$ A

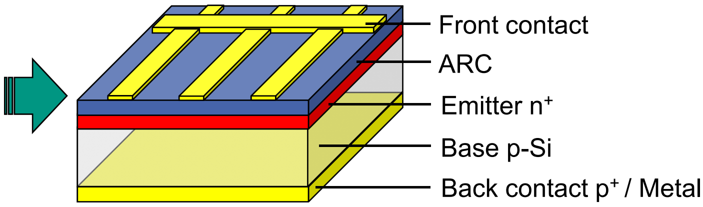
Screen Printed Solar Cells

Overview Production – Main Processes

Starting material:
- mc-Si (or Cz) Wafer
- 125 x 125 mm² or 150 x 150 mm²
- 200-340 µm thick



Solar Cells:
- 15-16% efficiency

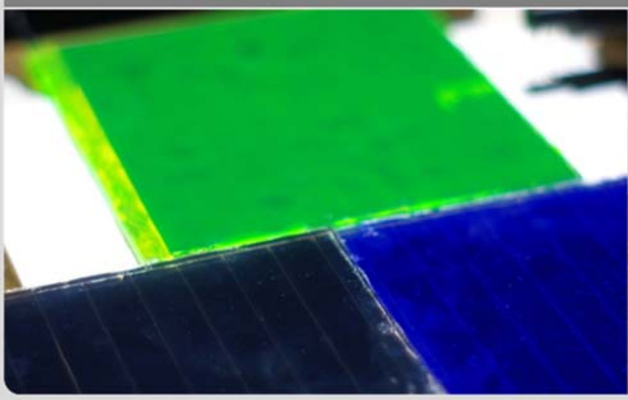


"Solar Energy" WS 2014/2015

Lecture 7:
Part 1: Fabrication of Silicon Solar Cells
Part 2: Thin Film Crystalline Silicon Solar Cells

Prof. Dr. Bryce S. Richards
Institute of Microstructure Technology (IMT), Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen
Light Technology Institute (LTI), Engesserstrasse 13, Building 30.34, 76131 Karlsruhe

KIT Focus Optics & Photonics



Thin Film Solar Cells

Why thin film?

- Very energy-intensive process growing MG-Si, and then either Cz c-Si or mc-Si ingots
- Significant losses during wafering process
- Solar cells end up inside a sheet of glass anyway, so why not use the glass as a substrate to deposit onto?
- With good light trapping $\Rightarrow$ don't need 300 μm of Si, 2 μm of semiconductor enough (even with Si)
- More uniform product appearance
- Higher throughput
- Demand for silicon exceeding supply
- So there should be a distinct cost advantage….

Thin Film Solar Cells

Why crystalline silicon thin film?

- No degradation like with amorphous silicon (a-Si) solar cells

… but still an indirect bandgap so excellent light trapping needed!

- Note that this is NOT single crystal silicon
  - actually small grain polycrystalline Si
  - also called micro-cystalline silicon (μc-Si)

Source: http://www.pressebox.de/pressemitteilung/csg-solar-ag/Dr-Ottmar-Koeder-wird-neues-Vorstandsmitglied-fuer-den-Bereich-Produktion-der-CSG-Solar-AG/boxid/186646

Thin Film c-Si Solar Cells

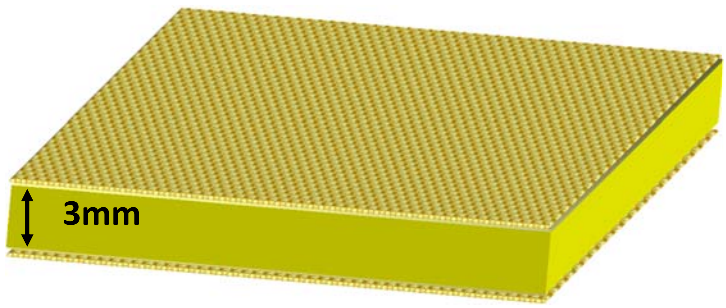
Karlsruher Institut für Technologie

Source: https://www.youtube.com/watch?v=2CGvMG1kuAo

CSG Solar: Fabrication Steps of Thin-Film Solar Cell

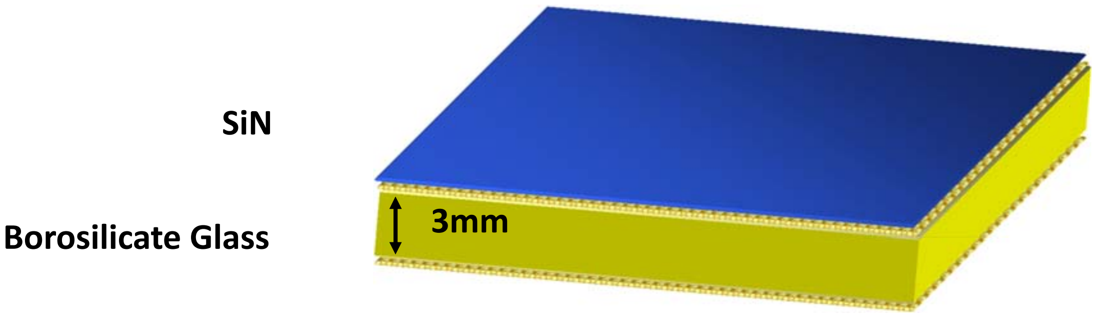
Karlsruher Institut für Technologie

Borosilicate Glass



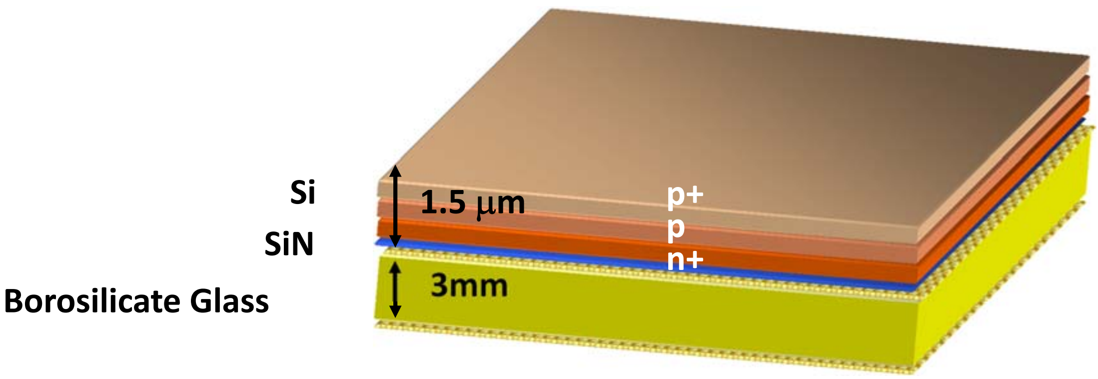
Texture Coat Both Surfaces (Dipping)

CSG Solar: Fabrication Steps of Thin-Film Solar Cell



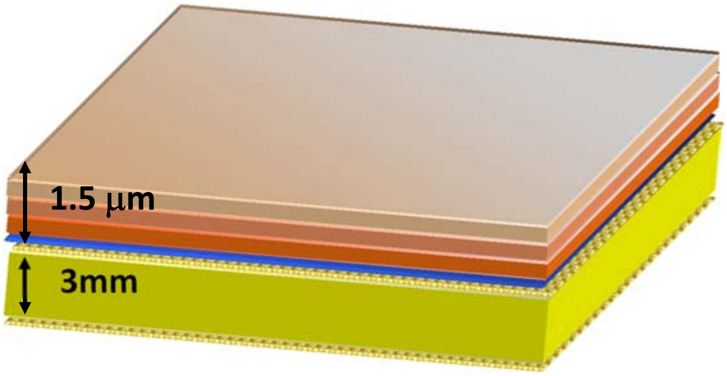
Deposit Anti-Reflection Coating (PECVD)

CSG Solar: Fabrication Steps of Thin-Film Solar Cell



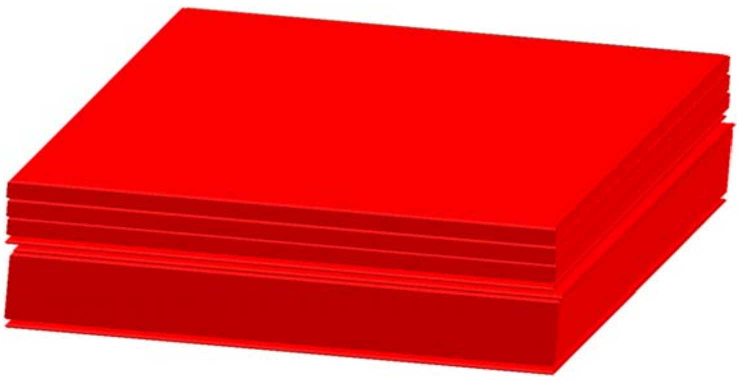
Deposit Silicon Film (PECVD)

CSG Solar: Fabrication Steps of Thin-Film Solar Cell



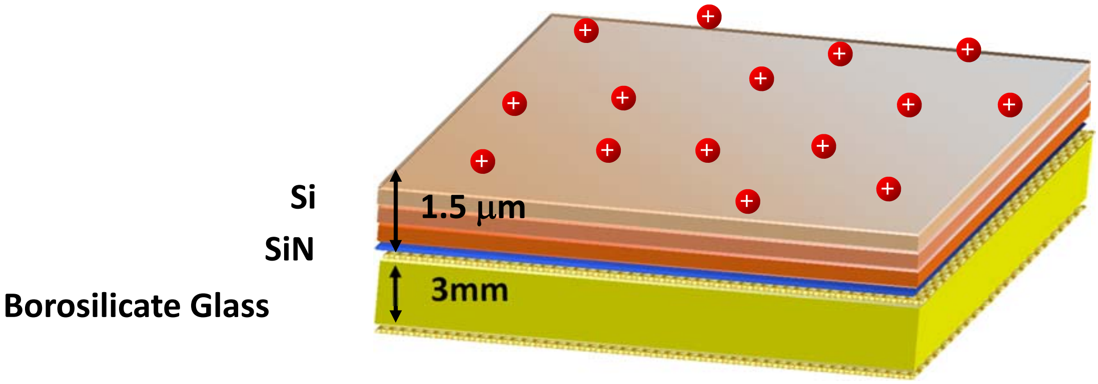
Crystallise Si

CSG Solar: Fabrication Steps of Thin-Film Solar Cell



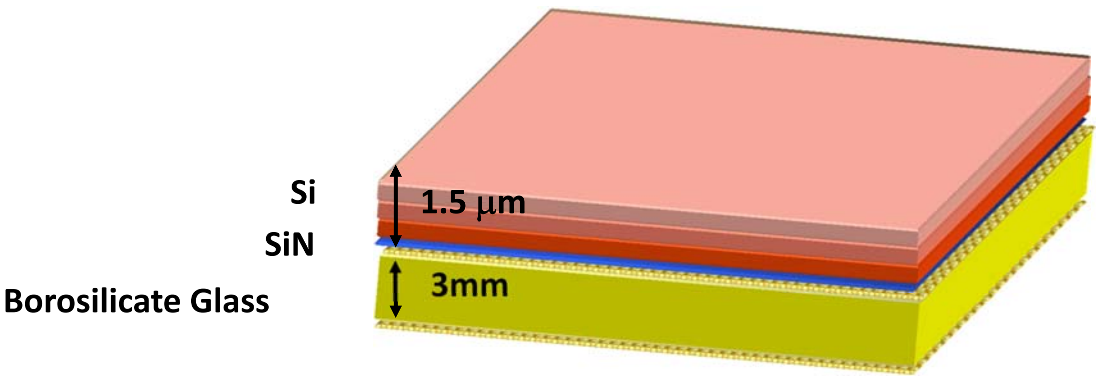
Anneal Defects

CSG Solar: Fabrication Steps of Thin-Film Solar Cell



Hydrogen Passivation

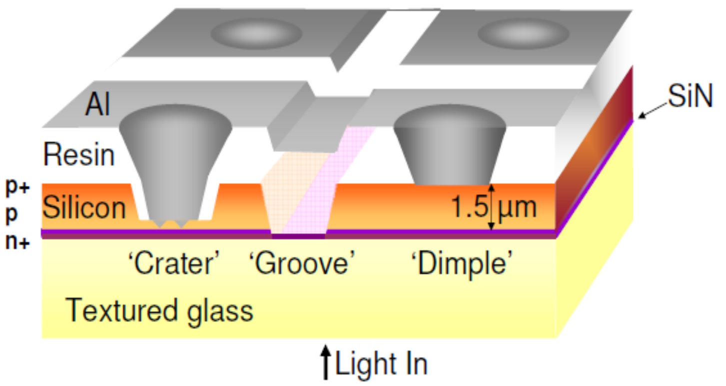
CSG Solar: Fabrication Steps of Thin-Film Solar Cell

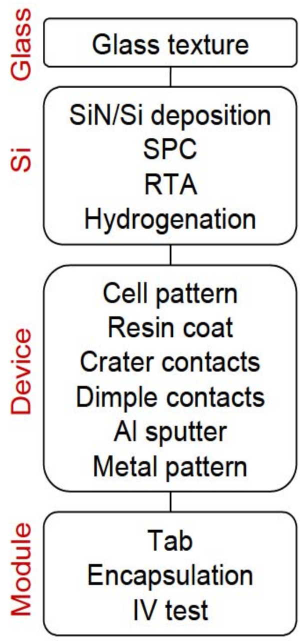


Hydrogen Passivation

CSG Solar: Fabrication Steps of Thin-Film Solar Cell

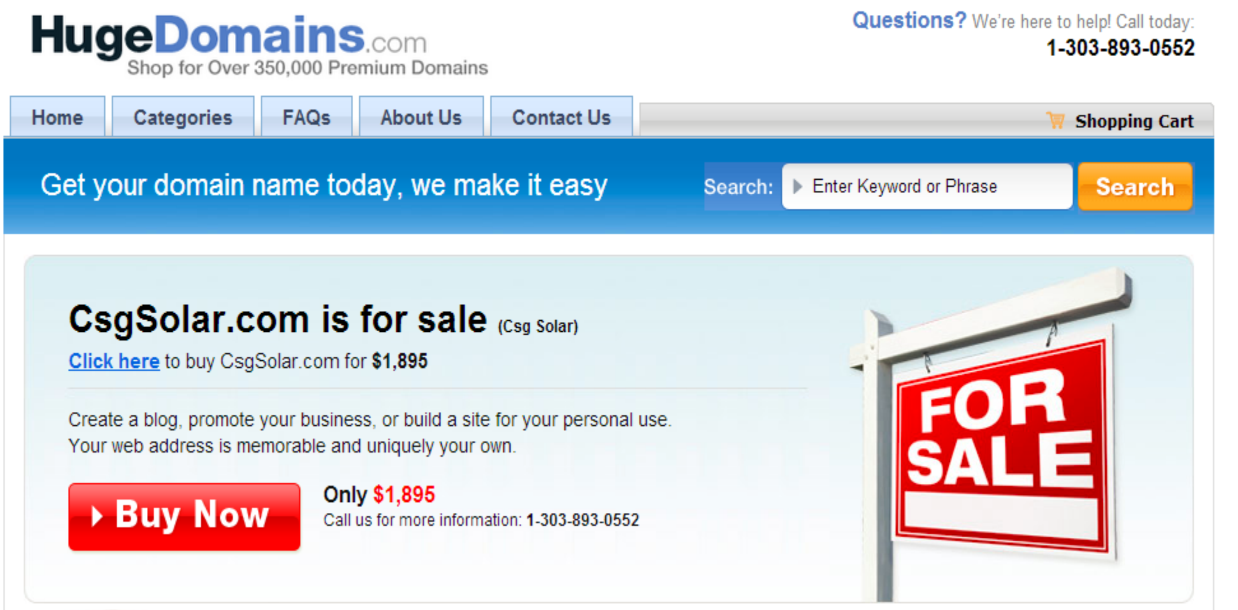
CSG module schematic





Quelle: www.csgsolar.com

www.csgsolar.com: Polykristalline Dünnschicht-Silizumzellen



Status am 19.11.2012

Suntech beendet Entwicklungsarbeiten bei Tochterunternehmen CSG Solar | 29.07.2011

Zurück zur Ausgangsseite

Die CSG Solar AG, Bitterfeld-Wolfen, stellt ihre Tätigkeit endgültig ein. Das teilt die Suntech Power Holdings Co., Ltd., Wuxi mit. Der chinesische Photovoltaikkonzern, der zu den führenden Herstellern von Solarmodulen auf der Basis kristalliner Solarzellen gehört, hatte das deutsche Unternehmen übernommen, nachdem es 2009 in Liquiditätsnot geraten war.

csgsolar

„Die Schließung von CSG wird es uns erlauben, uns besser darauf zu konzentrieren, was wir am besten können: Unsere Kunden weltweit mit leistungsstarken und zuverlässigen kristallinen Solarmodulen zu beliefern", sagt Dr. Zhengrong Shi, Chairman und CEO von Suntech.

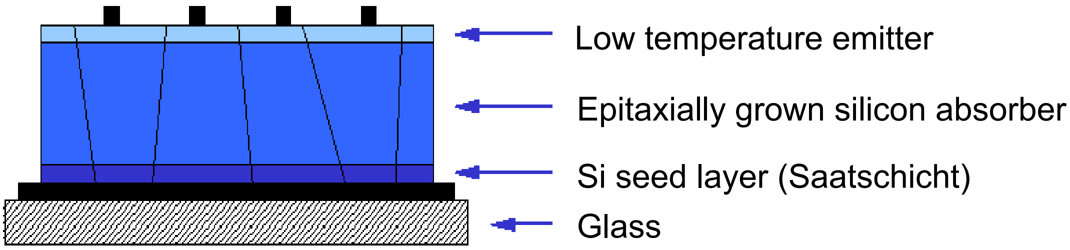
Die CSG Solar AG wurde 2004 durch ehemalige Mitarbeiter der Pacific Solar Inc., Sydney/Australien, gegründet. Das Unternehmen setzte auf eine Technologie, bei der auf Glas zunächst Siliziumnitrid als Antireflexionsschicht und dann nachfolgend Silizium in drei dünnen, unterschiedlich dotierten Schichten abgeschieden wird. Anschließend wurde das Silizium durch Erhitzen kristallisiert. Das brachte Kostenprobleme – nicht zuletzt deshalb, weil für dieses Verfahren hitzebeständiges Borosilikatglas benötigt wird, das deutlich teurer ist als das übliche Solarglas.

SUNTECH

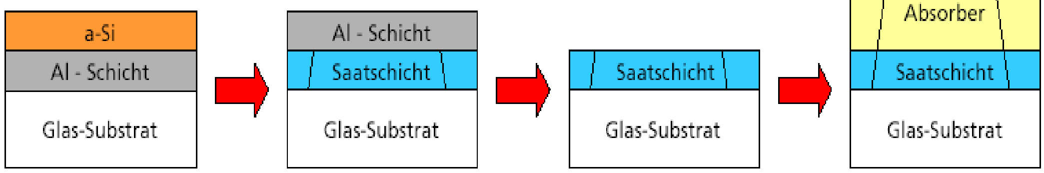
Auch die Strukturierung des Moduls sowie Rückseitenbeschichtung, die Durchkontaktierung und das Aufbringen der Leiterbahnen erfolgten mit einem relativ hohen technischen Aufwand. Dennoch erreichte CSG Solar seinerzeit lediglich einen Modulwirkungsgrad von 6,5 Prozent. Das Unternehmen hoffte aber, den Prozess, der von einer Forschergruppe um Prof. Martin Green an der University of New South Wales in Sydney entwickelt worden war, weiter optimieren und den Wirkungsgrad der Module binnen Jahresfrist auf über zehn Prozent steigern zu können. Die Tatsache, dass nunmehr auch Suntech nicht mehr bereit ist, Geld in diese Technologie zu investieren, deutet darauf hin, dass es nicht gelungen ist, das Verfahren wirtschaftlich zu gestalten.

Suntech Power Holdings

Towards Single-Crystal Silicon Thin-Film Solar Cells



Process of Helmholtz-Zentrum Berlin (HZB):
aluminium induced crystallisation



Also being pursued by Fraunhofer ISE

But does this solve the key problems….?

CSG Solar

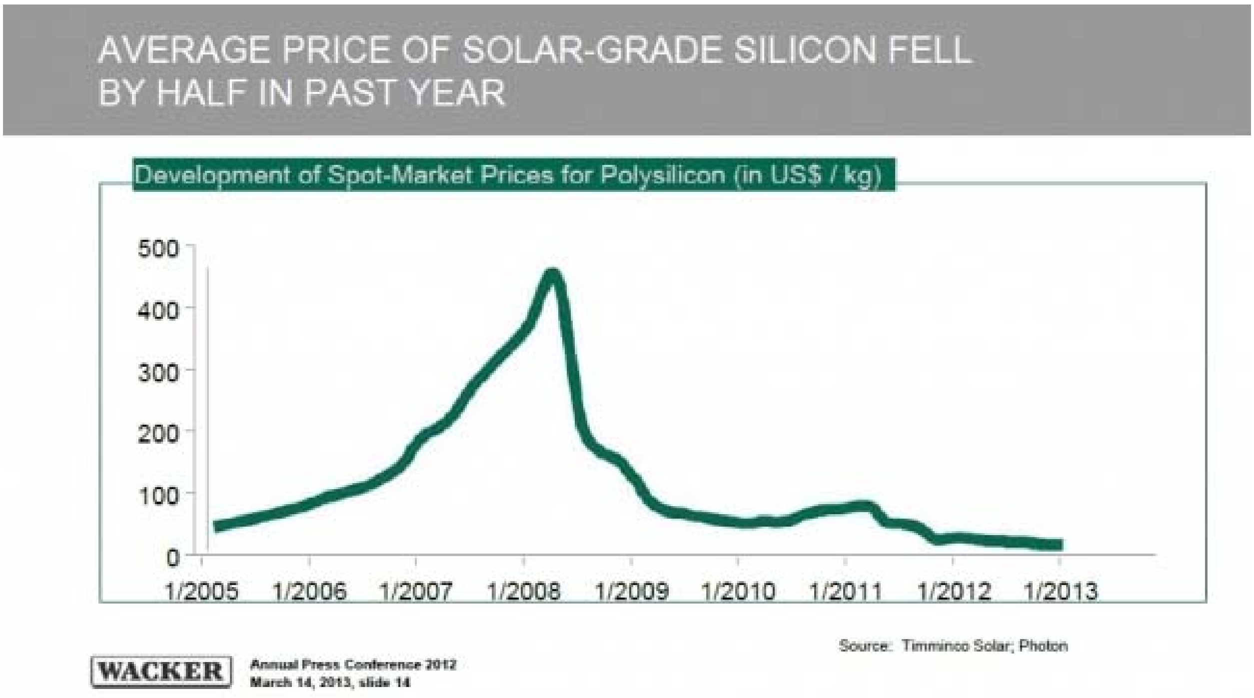
Why did it fail?

- Never got over 10% for full size (~1m^2) modules
- Cannot ignore the balance-of-systems (BoS) costs
  ⇒ remember from Dr. Goldschmidt's lecture that
  these are area-related
- Global recession started in 2009…. (reduced demand)

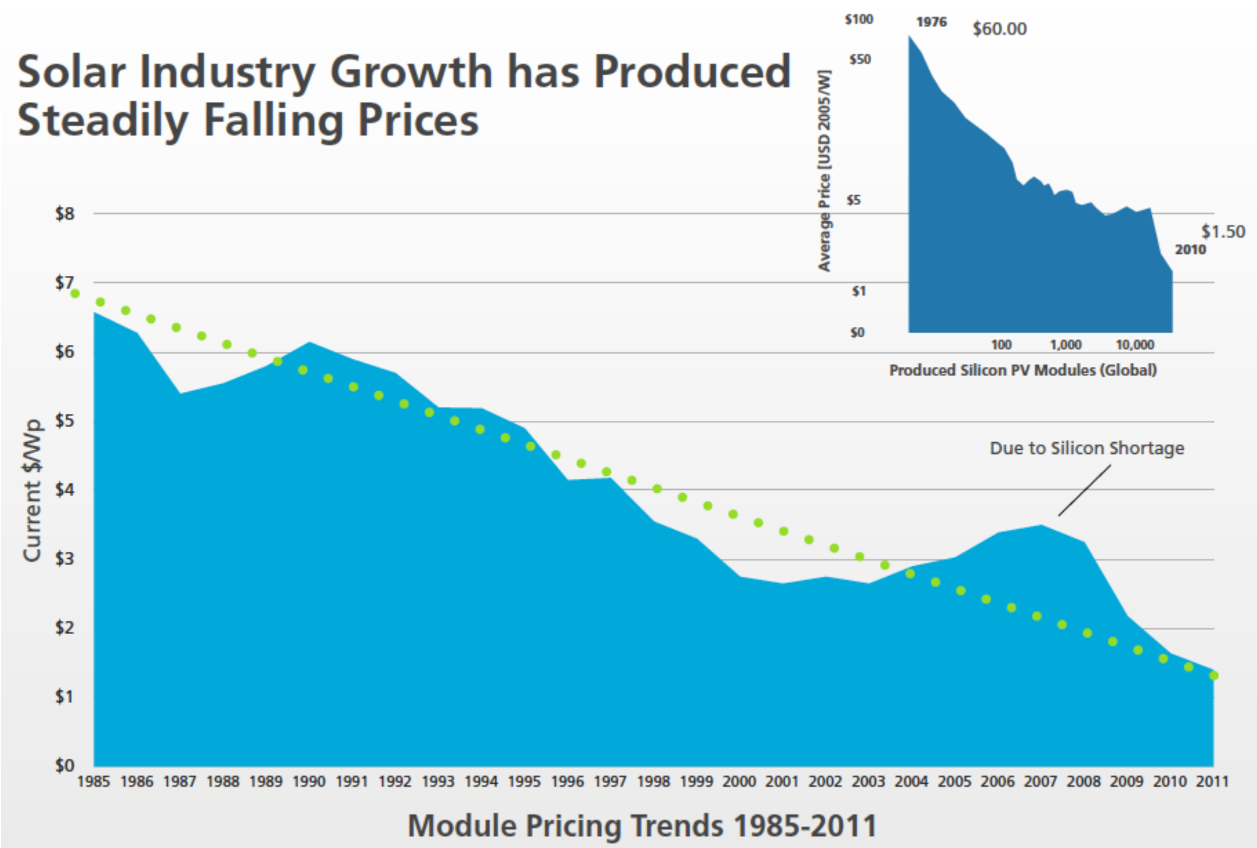
  … combined with huge amount of poly-Si manufacturing plants coming online (over supply)…

  … meant that the bottom dropped out of the wafer-based silicon solar market

Silicon Prices



Source: http://www.pv-tech.org/news/polysilicon_prices_at_wacker_fell_50_in_2012



Source: http://costofsolar.com/management/uploads/2013/12/solar-pv-cost-trend.png

Silicon Prices

PV Spot Price

【Annoucement】We've added new columns for mono-si module and high-efficiency/mono-si cell and adjusted standard for wafers. Any questions,please don't hesitate to[contact us] !

Price quotes updated weekly ($US)< Limitations on Liability > Methodology

Polysilicon

2014/11/12 update

Item	High	Low	Avg	Chg	Chart
Polysilicon Price (Per KG)	23.50	19.00	20.700	— (0 %)	

Wafer

2014/11/12 update

Item	High	Low	Avg	Chg	Chart
Super High Efficiency Multi-Si Wafer (156mm x 156mm) NEW	1.02	0.93	0.965	▲ (3.76 %)	
High Efficiency Multi-Si Wafer (156mm X 156mm) NEW	0.93	0.87	0.900	— (0 %)	
Mono-Si Wafer (156mm x 156mm)	1.20	1.10	1.155	▼ (-0.86 %)	

*The efficiency of cell made from super high-efficiency wafer is higher than mainstream product, thus its price is higher than mainstream wafer price.

Source: http://pv.energytrend.com/pricequotes.html

Silicon Prices

Cell

2014/11/12 update

Item	High	Low	Avg	Chg	Chart
High Efficiency Multi-Si Cell (Per Watt) NEW	0.43	0.33	0.340	— (0 %)	
Taiwanese Multi-Si Cell (Per Watt)	0.34	0.32	0.325	▼ (-1.52 %)	
Chinese Multi-Si Cell (Per Watt)	0.34	0.30	0.320	▲ (0.31 %)	
Mono-Si Cell (Per Watt) NEW	0.47	0.40	0.425	— (0 %)	
Mono-Si Cell with PERC (Per Watt)	become our MI member to access full data				

*The definition of high-efficiency multi-si cell is cell with efficiency above 17.8%.

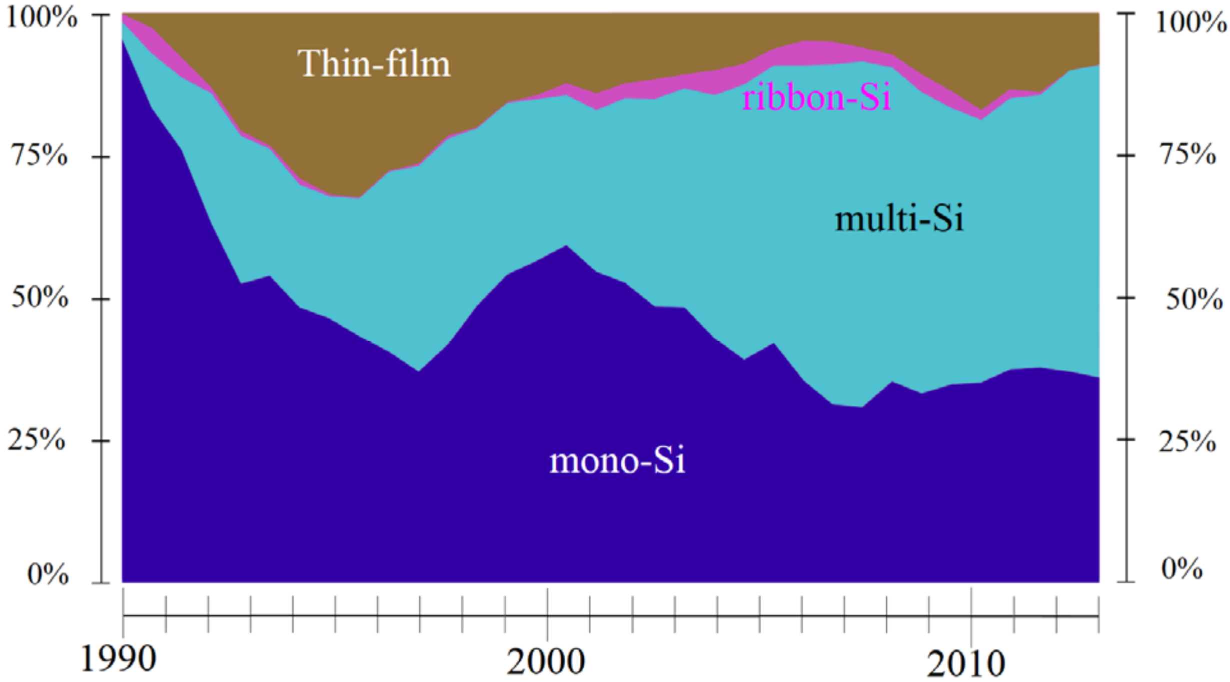
Module

2014/11/12 update

Item	High	Low	Avg	Chg	Chart
Multi-Si Module (Per Watt)	0.69	0.53	0.578	— (0 %)	
Mono-Si Module (Per Watt) NEW	0.74	0.61	0.630	— (0 %)	

Source: http://pv.energytrend.com/pricequotes.html

Silicon Market Share



Source: http://en.wikipedia.org/wiki/Thin_film_solar_cell

Summary

- Simple and robust fabrication process for screen-printed PV
- High energy intensity of crystalline silicon in general
- mc-Si and c-Si solar cells remain dominant – mostly lower-tech screen-printed devices
- Success of a technology has more to do with timing, the economic climate and what government policy in key countries around the world is doing than the technical merit $\Rightarrow$ frustrating for an engineer!
- Hence, wafer based Si presents all other technologies with a "moving goal post" $\Rightarrow$ always incrementally decreasing costs and increasing η $\Rightarrow$ technology expected to dominate for at least another decade